

**Remarks**

Claims 1-4 are pending in this action. Claims 1-4 stand rejected. By this amendment claim 1 has been amended. Applicants respectfully request reconsideration of all pending claims herein. No new matter has been added to the application by virtue of the present amendment.

**Certified Copies of Foreign Priority Documents**

Applicants have enclosed a certified copy of the foreign priority document JP2004-3021164 with this amendment, mailed February 7, 2006. The foreign priority document JP2004-3021164 was filed in the Japanese Patent Office on June 27, 2003.

**In the Drawings**

The Office Action stated an objection to the drawings as failing to comply with 37 CFR 1.84(p)(4) because reference characters "DI" and "ID" have both been used to designate data signal DI (figure 2). A proposed drawing to overcome the objection to Figure 2 is attached to this amendment as Appendix A. The proposed drawing is labeled "Replacement Sheet" to be in compliance with 37 CFR 1.121(d).

**In the Specification**

Applicants have amended paragraph 0056 lines 2-4 to clearly differentiate the corresponding latch circuits by assigning the correct reference characters. Applicants submit that the objection to the specification described in the Office Action has been overcome.

**Claim Rejections – 35 U.S.C. 102 (e)**

The Office Action has rejected claims 1-4 under 35 U.S.C. 102(e) as being anticipated by Morton. (U.S. Application No. 2004/0078741)

The Office Action states that claim 1 is rejected because Morton describes a first latch, which latches input data based on an incoming clock signal, and a second latch, which receives an output signal of the first latch. The Office Action also states that the second signal is complementary to the first signal based on the logic gates shown when the test signal is inactive.

Applicants respectfully submit that Morton does not anticipate applicant's claimed invention as amended because applicant's invention is a transparent latch circuit which behaves as a latch throughout the duration of a test as described in claim 1 as amended "[...]a first latch circuit for receiving a data signal and latching the data signal in response to at least one of a first signal fluctuating periodically and a test signal in the active state; a second latch circuit for receiving an output signal of said first latch circuit and latching the output signal of said first latch circuit in response to at least one of a second signal complementary to the first signal and the test signal in the active state [...]"(see Ueda Summary, paragraph 0043 lines 10-16, and figures 1-3).

The invention disclosed by Morton describes a circuit that, in test mode, first behaves as a latch then transitions to a transparent latch, and finally transitions back to a latch. Specifically, Morton teaches a latch circuit wherein a first latch is held in its latched state (see Morton paragraph 0034 lines 4-7 and Figure 7), and a second latch is temporarily put into its transparent state (see Morton paragraph 0036 lines 1-3, and Figure 7) then returned to its latched state (see Morton paragraphs 0037 lines 1-2, and Figure 7).

Furthermore, the invention described by Morton solves a hold-time problem in a scan chain

but cannot be used to solve the problem of how to include a transparent latch in an edge-sensitive scan chain as described in the instant application. Therefore, Applicant's respectfully submit that the invention taught by Morton does not anticipate Applicant's claimed invention as amended.

As noted above, Applicants have amended claim 1, and hence also claims 2-4 which depend from claim 1, to incorporate limitations cited in the specification that patentably distinguish the Morton reference cited by the Office Action. Accordingly, Applicants respectfully submit that the rejection of claims 1-4 under 35 U.S.C. § 102(e) has been overcome. Therefore Applicant respectfully submits that all claims are in condition for allowance.

**Summary and Conclusion**

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,

For: Ueda

By: 

William D. Sabo

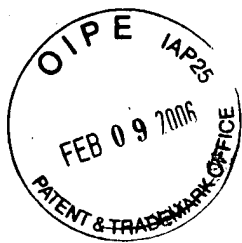
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## Appendix A

### Replacement Drawing (1 sheet)